# JM434D643A-60

**200PIN DDR333 Unbuffered SO-DIMM**
**256MB With 32Mx8 CL2.5**

## Description

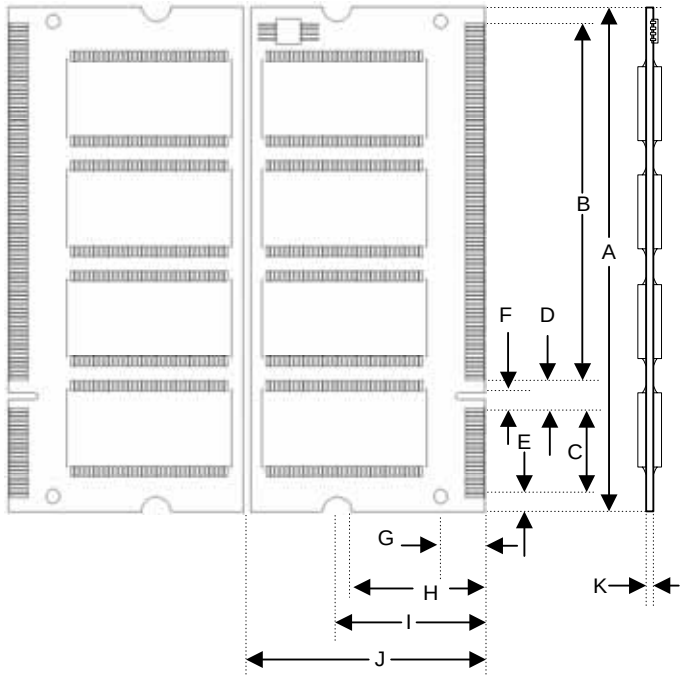
The JM434D643A-60 is a 32M x 64bits Double Data Rate SDRAM high-density for DDR333. The JM434D643A-60 consists of 8pcs CMOS 32Mx8 bits Double Data Rate SDRAMs in 66 pin TSOP-II 400mil packages, and a 2048 bits serial EEPROM on a 200-pin printed circuit board. The JM434D643A-60 is a Dual In-Line Memory Module and is intended for mounting into 200-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

## Features

- Power supply: VDD: 2.5V ± 0.2V, VDDQ: 2.5V ± 0.2V
- Max clock Freq: 166MHZ.
- Double-data-rate architecture; two data transfers per clock cycle
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transition with CK transition
- Auto and Self Refresh 7.8us refresh interval.
- Data I/O transactions on both edge of data strobe.
- Edge aligned data output, center aligned data input.
- Serial Presence Detect (SPD) with serial EEPROM
- SSTL-2 compatible inputs and outputs.
- MRS cycle with address key programs.
  - CAS Latency (Access from column address) : 2.5
  - Burst Length (2,4,8 )
  - Data Sequence (Sequential & Interleave)

## Placement




**PCB: 09-1220**

## Dimensions

| Side | Millimeters | Inches |
|---|---|---|
| A | 67.60±0.20 | 2.661±0.008 |
| B | 47.40 | 1.866 |
| C | 11.40 | 0.449 |
| D | 4.20 | 0.165 |
| E | 2.15 | 0.085 |
| F | 1.80 | 0.071 |
| G | 6.00 | 0.236 |
| H | 18.00 | 0.709 |
| I | 20.00 | 0.787 |
| J | 31.75±0.20 | 1.250±0.008 |
| K | 1.00±0.10 | 0.039±0.004 |

**(Refer Placement)**

## Pin Identification

| Symbol | Function |
|---|---|
| A0~A12, BA0, BA1 | Address input |
| DQ0~DQ63 | Data Input / Output. |
| DQS0~DQS7 | Data strobe input/output |
| CK0~CK1 | Clock Input. |
| /CK0~CK1 | |
| CKE0 | Clock Enable Input. |
| /CS0 | Chip Select Input. |
| /RAS | Row Address Strobe |
| /CAS | Column Address Strobe |
| /WE | Write Enable |
| DM0~DM7 | Data-in Mask |
| VDD | +2.5 Voltage power supply |
| VDDQ | +2.5 Voltage Power Supply for DQS |
| VREF | Power Supply for Reference |
| VDDSPD | +2.5 Voltage Serial EEPROM |
| | Power Supply |
| SA0~SA2 | Address in EEPROM |
| SCL | Serial PD Clock |
| SDA | Serial PD Add/Data input/output |
| VSS | Ground |
| NC | No Connection |

**Pinouts:**

| Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01 | VREF | 69 | VDD | 137 | VSS | 02 | VREF | 70 | VDD | 138 | VSS |
| 03 | VSS | 71 | *CB0 | 139 | DQ35 | 04 | VSS | 72 | *CB4 | 140 | DQ39 |
| 05 | DQ0 | 73 | *CB1 | 141 | DQ40 | 06 | DQ4 | 74 | *CB5 | 142 | DQ44 |
| 07 | DQ1 | 75 | VSS | 143 | VDD | 08 | DQ5 | 76 | VSS | 144 | VDD |
| 09 | VDD | 77 | *DQS8 | 145 | DQ41 | 10 | VDD | 78 | *DM8 | 146 | DQ45 |
| 11 | DQS0 | 79 | *CB2 | 147 | DQS5 | 12 | DM0 | 80 | *CB6 | 148 | DM5 |
| 13 | DQ2 | 81 | VDD | 149 | VSS | 14 | DQ6 | 82 | VDD | 150 | VSS |
| 15 | VSS | 83 | *CB3 | 151 | DQ42 | 16 | VSS | 84 | *CB7 | 152 | DQ46 |
| 17 | DQ3 | 85 | DU | 153 | DQ43 | 18 | DQ7 | 86 | DU | 154 | DQ47 |
| 19 | DQ8 | 87 | VSS | 155 | VDD | 20 | DQ12 | 88 | VSS | 156 | VDD |
| 21 | VDD | 89 | *CK2 | 157 | VDDD | 22 | VDD | 90 | VSS | 158 | /CK1 |
| 23 | DQ9 | 91 | */CK2 | 159 | VSS | 24 | DQ13 | 92 | VDD | 160 | CK1 |
| 25 | DQS1 | 93 | VDD | 161 | VSS | 26 | DM1 | 94 | VDD | 162 | VSS |
| 27 | VSS | 95 | *CKE1 | 163 | DQ48 | 28 | VSS | 96 | CKE0 | 164 | DQ52 |
| 29 | DQ10 | 97 | *A13 | 165 | DQ49 | 30 | DQ14 | 98 | DU | 166 | DQ53 |
| 31 | DQ11 | 99 | *A12 | 167 | VDD | 32 | DQ15 | 100 | A11 | 168 | VDD |
| 33 | VDD | 101 | A9 | 169 | DQS6 | 34 | VDD | 102 | A8 | 170 | DM6 |
| 35 | CK0 | 103 | VSS | 171 | DQ50 | 36 | VDD | 104 | VSS | 172 | DQ54 |
| 37 | /CK0 | 105 | A7 | 173 | VSS | 38 | VSS | 106 | A6 | 174 | VSS |
| 39 | VSS | 107 | A5 | 175 | DQ51 | 40 | VSS | 108 | A4 | 176 | DQ55 |
| 41 | DQ16 | 109 | A3 | 177 | D56 | 42 | DQ20 | 110 | A2 | 178 | DQ60 |
| 43 | DQ17 | 111 | A1 | 179 | VDD | 44 | DQ21 | 112 | A0 | 180 | VDD |
| 45 | VDD | 113 | VDD | 181 | DQ57 | 46 | VDD | 114 | VDD | 182 | DQ61 |
| 47 | DQS2 | 115 | A10 | 183 | DQS7 | 48 | DM2 | 116 | BA1 | 184 | DM7 |
| 49 | DQ18 | 117 | BA0 | 185 | VSS | 50 | DQ22 | 118 | /RAS | 186 | VSS |
| 51 | VSS | 119 | /WE | 187 | DQ58 | 52 | VSS | 120 | /CAS | 188 | DQ62 |
| 53 | DQ19 | 121 | /CS0 | 189 | DQ59 | 54 | DQ23 | 122 | */CS1 | 190 | DQ63 |
| 55 | DQ24 | 123 | DU | 191 | VDD | 56 | DQ28 | 124 | DU | 192 | VDD |
| 57 | VDD | 125 | VSS | 193 | SDA | 58 | VDD | 126 | VSS | 194 | SA0 |
| 59 | DQ25 | 127 | DQ32 | 195 | SCL | 60 | DQ29 | 128 | DQ36 | 196 | SA1 |
| 61 | DQS3 | 129 | DQ33 | 197 | VDDSPD | 62 | DM3 | 130 | DQ37 | 198 | SA2 |
| 63 | VSS | 131 | VDD | 199 | VDD | 64 | VSS | 132 | VDD | 200 | DU |
| 65 | DQ26 | 133 | DQS4 | | | 66 | DQ30 | 134 | DM4 | | |
| 67 | DQ27 | 135 | DQ34 | | | 68 | DQ31 | 136 | DQ38 | | |